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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,156	03/25/2004	Chung-Hsiao R. Wu	5681-72600	7383

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EXAMINER	
CHANG, ERIC	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,156	WU, CHUNG-HSIAO R.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2-24-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are pending.

Claim Objections

2. Claim 8 is objected to because of the following informalities: the term "form" on line 2 of the claim should read, "from". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Description of the Related Art section in the Applicant's Specification, hereafter Applicant's Admitted Prior Art, in view of U.S. Patent 6,850,554 to Sha et al.

5. As to claim 1, Applicant's Admitted Prior Art discloses a clock board for a redundant clock distribution system, the clock board comprising: a clock synthesizer configured to provide an input clock signal, wherein energy of the input clock signal is substantially concentrated around an input clock signal frequency [page 1, lines 14-19].

Applicant's Admitted Prior Art teaches the limitations of the claim, including that electromagnetic interference is a problem with clock boards [page 1, lines 21-25], but does not teach that a spread spectrum unit coupled to receive the input clock signal from the clock synthesizer, wherein the spread spectrum unit is configured to frequency modulate the input clock signal, thereby producing an output clock signal, wherein energy of the output clock signal is spread over a range of frequencies, and wherein, when the clock board is operating as a master in a redundant clock distribution system having a master clock board and a slave clock board, the spread spectrum unit is enabled.

Sha teaches that electromagnetic interference is a problem with clocking systems in electronic devices [col. 1, lines 26-30]. Thus, Sha teaches a clocking system similar to that of Applicant's Admitted Prior Art. Sha further teaches a spread spectrum unit is coupled to a clock synthesizer and configured to frequency modulate the input clock signal, thereby producing an output clock signal, wherein energy of the output clock signal is spread over a range of frequencies [col. 1, lines 31-40].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ a spread spectrum unit as taught by Sha. One of ordinary skill in the art would have been motivated to do so that the electromagnetic interference in the computer system is reduced.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of clocking computer systems. Moreover, the spread spectrum means taught by Sha would the efficiency of Applicant's Admitted Prior Art because it allowed the spread spectrum unit to be turned off when it is not

needed [col. 1, lines 59-67], for example, when its associated clock board is not the master clock board.

6. As to claim 2, Sha discloses the range of frequencies is centered around the input clock signal frequency [col. 1, lines 41-42].

7. As to claim 3, Sha discloses the range of frequencies extends from the input clock signal frequency down to a lower frequency [col. 1, lines 49-53].

8. As to claim 4, Sha discloses the range of frequencies is a predetermined is based on a percentage of the input clock signal frequency [col. 1, lines 49-55].

9. As to claim 5, Sha discloses the predetermined percentage is programmable [col. 2, lines 25-30].

10. As to claim 6, Applicant's Admitted Prior Art discloses a clock board can be configured to operate as the slave in the redundant clock distribution system [page 1, lines 14-19]. Sha teaches the spread spectrum unit is turned off when it is not needed [col. 1, lines 59-67]. It would have been obvious to one of ordinary skill in the art that when the clock board is not the primary clock board, the spread spectrum unit is not needed and therefore may be disabled.

11. As to claim 7, Sha discloses the spread spectrum unit is coupled to provide the output clock signal to a computer system [FIG. 3]. It is well known in the art that a computer system comprises buffers configured to couple clock signals to clocked circuits [col. 3, lines 25-28].

12. As to claim 8, Sha discloses the clock synthesizer is coupled to receive a feedback clock signal from the clock buffer [177].

13. As to claim 9, Sha discloses the clock board is presented with a clock signal [col. 3, lines 13-15], and the clock synthesizer is coupled to receive the clock signal [102]. It is well known in the art that a crystal is used to generate clock signals.

14. As to claims 10-11, Applicant's Admitted Prior Art discloses the clock synthesizer is configured to receive a reference clock signal from another clock board [page 1, lines 18-19]. Applicant's Admitted Prior Art teaches that clock boards can detect the failure of other clock boards to present a clock signal. Conversely, Applicant's Admitted Prior Art also therefore teaches that a clock board is configured to provide a reference clock signal to another clock board.

15. As to claim 12, Applicant's Admitted Prior Art discloses a computer system comprising: a plurality of clocked circuits [page 1, lines 8-9]; a first clock board coupled to the plurality of clocked circuits [page 1, lines 14-19]; and a second clock board coupled to the plurality of clocked circuits [page 1, lines 14-19]; wherein each of the first and second clock boards includes

a clock synthesizer configured to provide an input clock signal [page 1, lines 14-19], wherein the first clock board is configured to operate as a master clock board and the second clock board is configured to act as a slave clock board [page 1, lines 14-19], and wherein, responsive to a failure of the first clock board, the second clock board is configured to operate as the master clock board [page 1, lines 14-19].

Sha teaches a spread spectrum unit is coupled to a clock synthesizer and configured to frequency modulate the input clock signal, thereby producing an output clock signal, wherein energy of the output clock signal is spread over a range of frequencies [col. 1, lines 31-40], substantially concentrated around an input clock signal frequency [col. 1, lines 41-42], Sha further teaches the spread spectrum unit is turned off when it is not needed [col. 1, lines 59-67]. It would have been obvious to one of ordinary skill in the art that when the clock board is not the primary clock board, the spread spectrum unit is not needed and therefore may be disabled.

16. As to claim 13, Sha discloses the range of frequencies is centered around the input clock signal frequency [col. 1, lines 41-42].

17. As to claim 14, Sha discloses the range of frequencies extends from the input clock signal frequency down to a lower frequency [col. 1, lines 49-53].

18. As to claim 15, Sha discloses the range of frequencies is based on a predetermined percentage of the input clock signal frequency [col. 1, lines 49-55].

19. As to claim 16, Sha discloses the predetermined percentage is programmable [col. 2, lines 25-30].

20. As to claim 17, Sha discloses spread spectrum units are coupled to provide the output clock signal to a computer system [FIG. 3]. It is well known in the art that a computer system comprises buffers configured to couple clock signals to clocked circuits [col. 3, lines 25-28].

21. As to claim 18, Applicant's Admitted Prior Art discloses each of the first and second clock boards is coupled to provide its respective output clock signal to clocked circuits in the computer system [page 1, lines 14-19].

22. As to claims 19 and 21, Applicant's Admitted Prior Art discloses the clock synthesizer is configured to receive a reference clock signal from another clock board [page 1, lines 18-19]. Applicant's Admitted Prior Art teaches that clock boards can detect the failure of other clock boards to present a clock signal. Conversely, Applicant's Admitted Prior Art also therefore teaches that a clock board is configured to provide a reference clock signal to another clock board.

23. As to claim 20, Sha discloses the clock board is presented with a clock signal [col. 3, lines 13-15], and the clock synthesizer is coupled to receive the clock signal [102]. It is well known in the art that a crystal is used to generate clock signals.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

March 15, 2007
ec

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
4/2/07